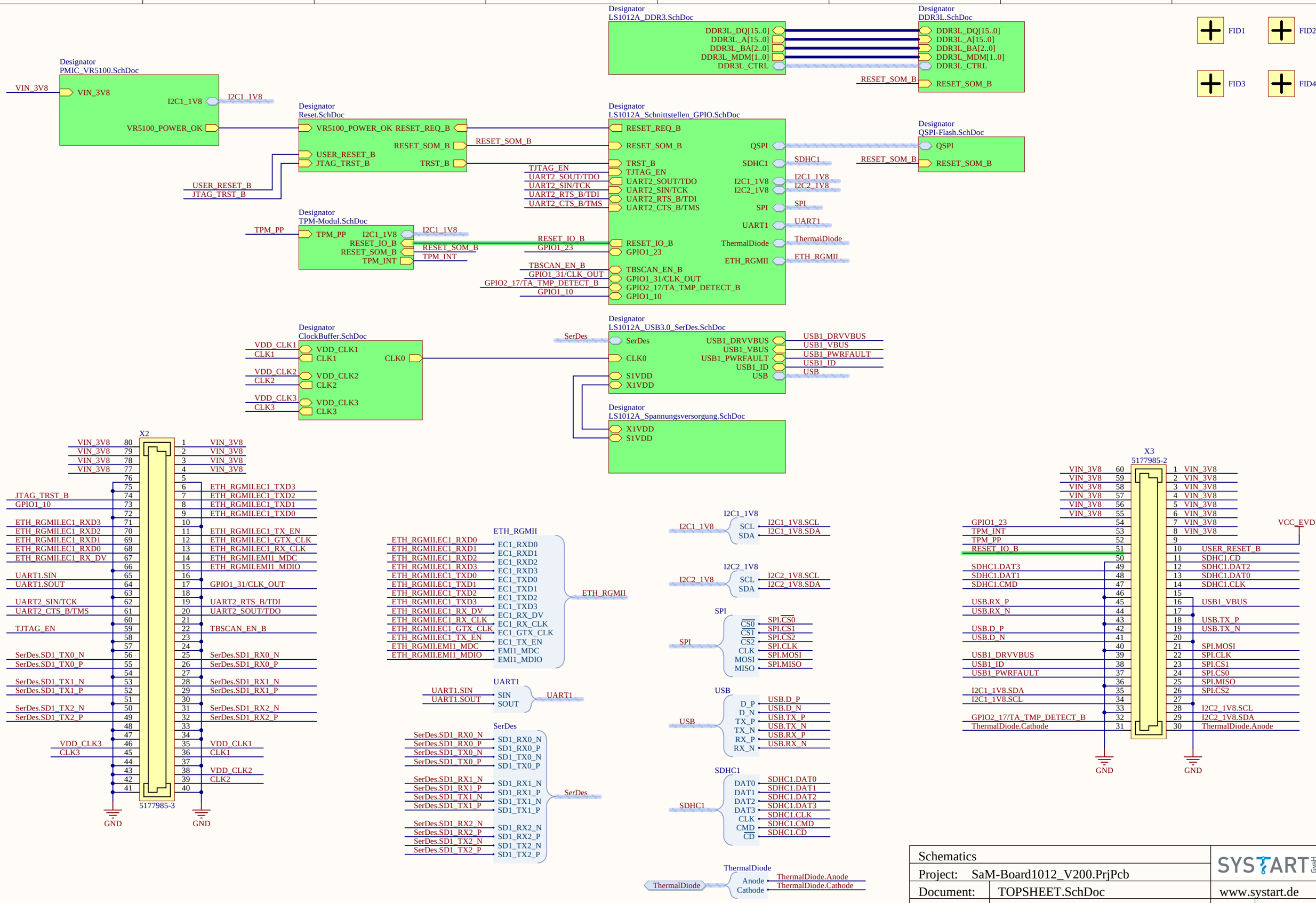
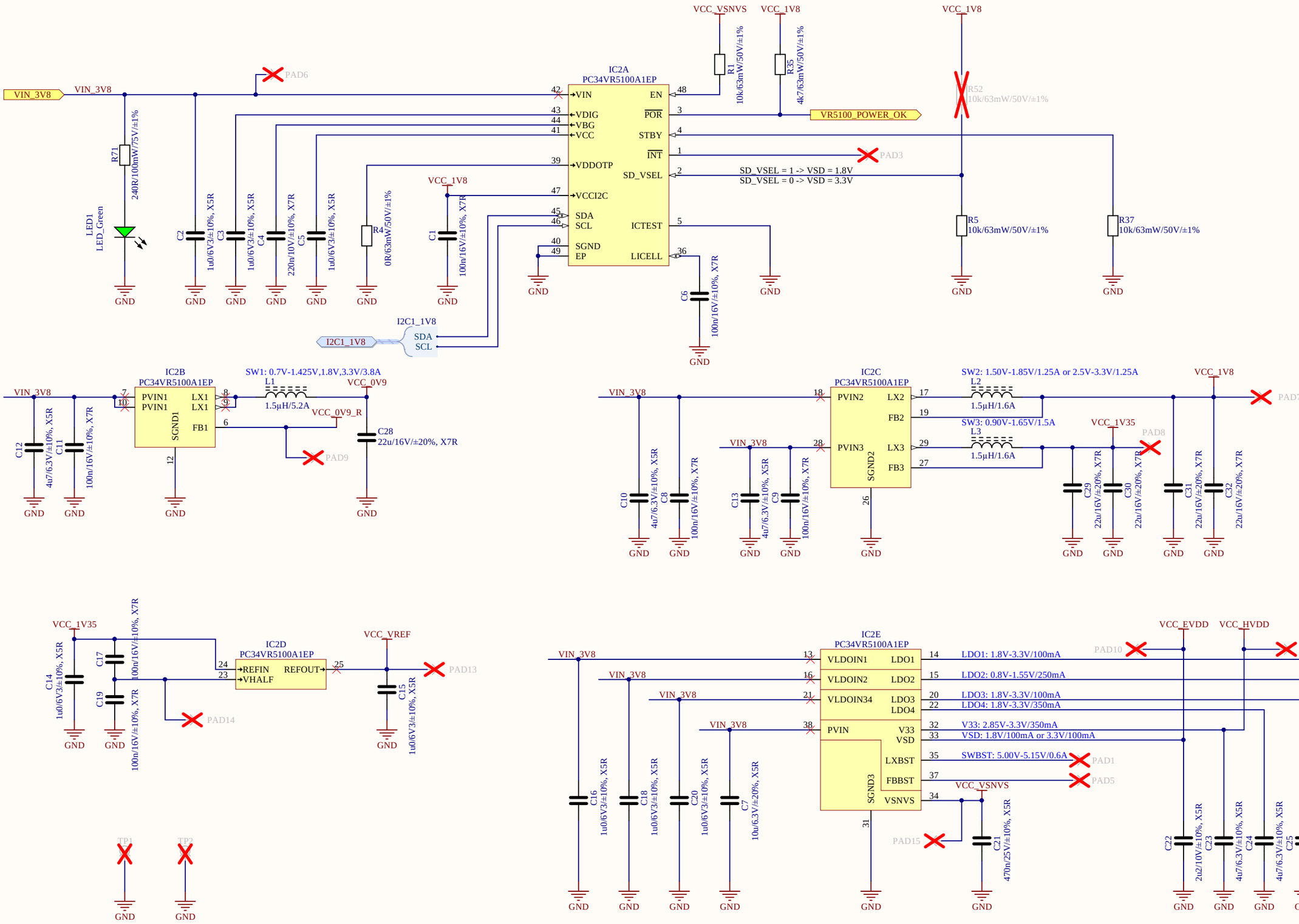
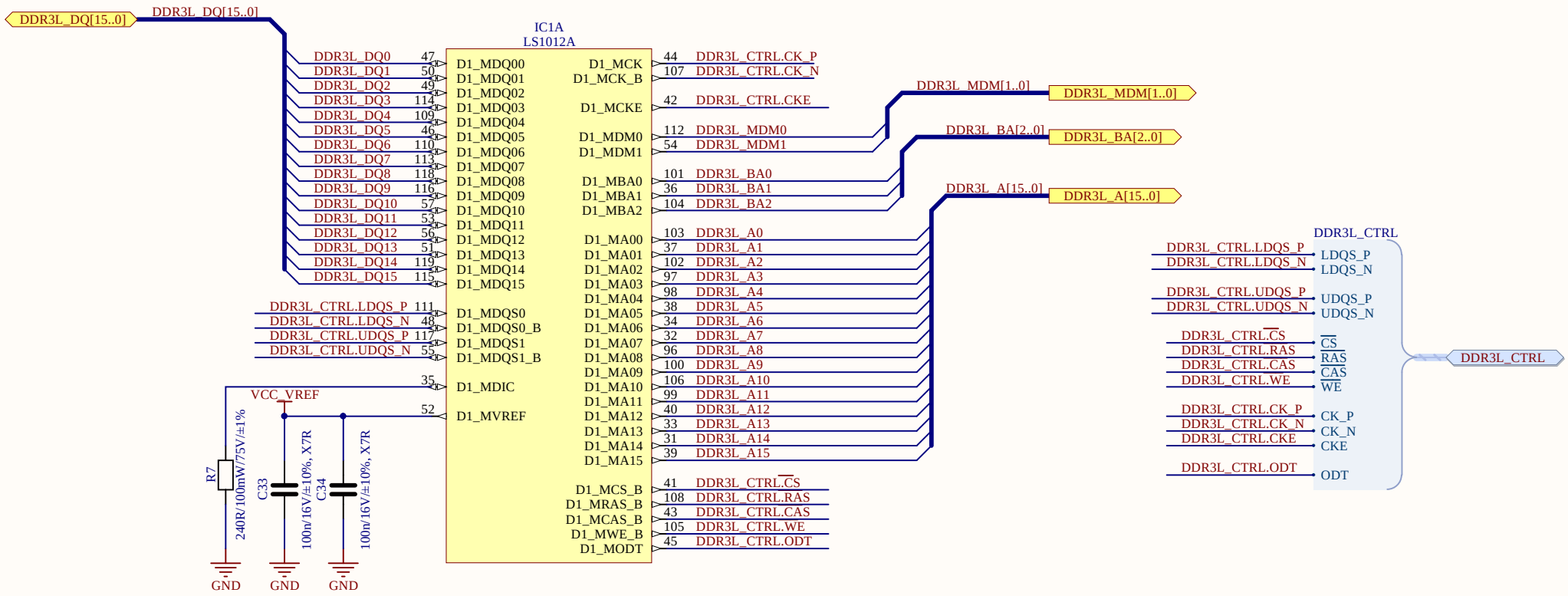

Designator
LS1012A_DDR3.SchDoc
DDR3L_DQ[15..0]
DDR3L_A[15..0]
DDR3L_BA[2..0]
DDR3L_MDM[1..0]
DDR3L_CTRL
RESET_SOM_B
Designator
DDR3L.SchDoc
DDR3L_DQ[15..0]
DDR3L_A[15..0]
DDR3L_BA[2..0]
DDR3L_MDM[1..0]
DDR3L_CTRL
RESET_SOM_B
FID1
FID2
FID3
FID4
Designator
PMIC_VR5100.SchDoc
VIN_3V8
I2C1_1V8
VR5100_POWER_OK
Designator
Reset.SchDoc
VR5100_POWER_OK
RESET_REQ_B
RESET_SOM_B
USER_RESET_B
JTAG_TRST_B
TRST_B
Designator
LS1012A_Schnittstellen_GPIO.SchDoc
RESET_REQ_B
RESET_SOM_B
TRST_B
TJTAG_EN
UART2_SOUT/TDO
UART2_SIN/TCK
UART2_RTS_B/TDI
UART2_CTS_B/TMS
QSPI
SDHC1
I2C1_1V8
I2C2_1V8
SPI
UART1
ThermalDiode
ETH_RGMII
RESET_IO_B
GPIO1_23
TBSCAN_EN_B
GPIO1_31/CLK_OUT
GPIO2_17/TA_TMP_DETECT_B
GPIO1_10
Designator
QSPI-Flash.SchDoc
QSPI
RESET_SOM_B
Designator
TPM-Modul.SchDoc
TPM_PP
I2C1_1V8
RESET_IO_B
RESET_SOM_B
TPM_INT
Designator
ClockBuffer.SchDoc
VDD_CLK1
CLK1
CLK0
VDD_CLK2
CLK2
VDD_CLK3
CLK3
Designator
LS1012A_USB3.0_SerDes.SchDoc
SerDes
CLK0
S1VDD
X1VDD
USB1_DRVVBUS
USB1_VBUS
USB1_PWRFAULT
USB1_ID
USB
Designator
LS1012A_Spannungsversorgung.SchDoc
X1VDD
S1VDD
X2
5177985-3
VIN_3V8
ETH_RGMII.EC1_TXD3
ETH_RGMII.EC1_TXD2
ETH_RGMII.EC1_TXD1
ETH_RGMII.EC1_TXD0
ETH_RGMII.EC1_TX_EN
ETH_RGMII.EC1_GTX_CLK
ETH_RGMII.EC1_RX_CLK
ETH_RGMII.EMI1_MDC
ETH_RGMII.EMI1_MDIO
JTAG_TRST_B
GPIO1_10
ETH_RGMII.EC1_RXD3
ETH_RGMII.EC1_RXD2
ETH_RGMII.EC1_RXD1
ETH_RGMII.EC1_RXD0
ETH_RGMII.EC1_RX_DV
UART1.SIN
UART1.SOUT
UART2_SIN/TCK
UART2_CTS_B/TMS
TJTAG_EN
SerDes.SD1_TX0_N
SerDes.SD1_TX0_P
SerDes.SD1_TX1_N
SerDes.SD1_TX1_P
SerDes.SD1_TX2_N
SerDes.SD1_TX2_P
SerDes.SD1_RX0_N
SerDes.SD1_RX0_P
SerDes.SD1_RX1_N
SerDes.SD1_RX1_P
SerDes.SD1_RX2_N
SerDes.SD1_RX2_P
VDD_CLK3
CLK3
VDD_CLK1
CLK1
VDD_CLK2
CLK2
GND
ETH_RGMII
EC1_RXD0
EC1_RXD1
EC1_RXD2
EC1_RXD3
EC1_TXD0
EC1_TXD1
EC1_TXD2
EC1_TXD3
EC1_RX_DV
EC1_RX_CLK
EC1_GTX_CLK
EC1_TX_EN
EMI1_MDC
EMI1_MDIO
UART1
SIN
SOUT
SerDes
SD1_RX0_N
SD1_RX0_P
SD1_TX0_N
SD1_TX0_P
SD1_RX1_N
SD1_RX1_P
SD1_TX1_N
SD1_TX1_P
SD1_RX2_N
SD1_RX2_P
SD1_TX2_N
SD1_TX2_P
I2C1_1V8
SCL
SDA
I2C1_1V8.SCL
I2C1_1V8.SDA
I2C2_1V8
I2C2_1V8.SCL
I2C2_1V8.SDA
SPI
CS0
CS1
CS2
CLK
MOSI
MISO
SPI.CS0
SPI.CS1
SPI.CS2
SPI.CLK
SPI.MOSI
SPI.MISO
USB
D_P
D_N
TX_P
TX_N
RX_P
RX_N
USB.D_P
USB.D_N
USB.TX_P
USB.TX_N
USB.RX_P
USB.RX_N
SDHC1
DAT0
DAT1
DAT2
DAT3
CLK
CMD
CD
SDHC1.DAT0
SDHC1.DAT1
SDHC1.DAT2
SDHC1.DAT3
SDHC1.CLK
SDHC1.CMD
SDHC1.CD
ThermalDiode
Anode
Cathode
ThermalDiode.Anode
ThermalDiode.Cathode
X3
5177985-2
VCC_EVDD
USER_RESET_B
SDHC1.CD
SDHC1.DAT2
SDHC1.DAT0
SDHC1.CLK
USB1_VBUS
USB.TX_P
USB.TX_N
SPI.MOSI
SPI.CLK
SPI.CS1
SPI.CS0
SPI.MISO
SPI.CS2
I2C2_1V8.SCL
I2C2_1V8.SDA
ThermalDiode.Anode
GND
Schematics
Project: SaM-Board1012_V200.PrjPcb
Document: TOPSHEET.SchDoc
Author: SAM
Date: 17.11.2017
Auditor: MSB
Date: 18.11.2017
Status: Confirmed
Page: 1
SYSTART GmbH
www.systart.de



Schematics		SYSTART GmbH	
Project: SaM-Board1012_V200.PrjPcb			
Document:	PMIC_VR5100.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
Status:	Confirmed	Page:	2



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Document:	LS1012A_DDR3.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
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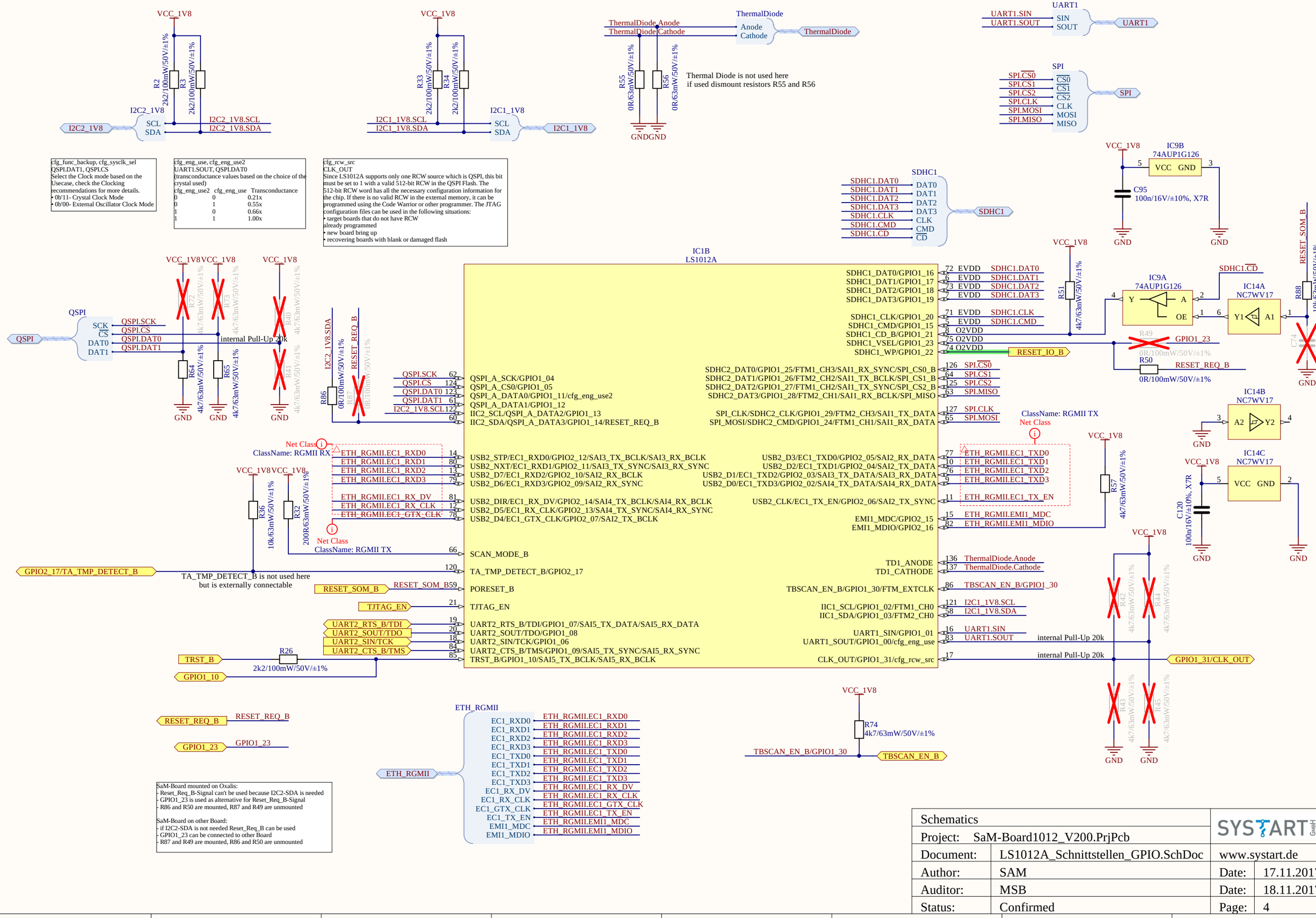

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Project: SaM-Board1012_V200.PrjPcb			
Document:	LS1012A_Schnittstellen_GPIO.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
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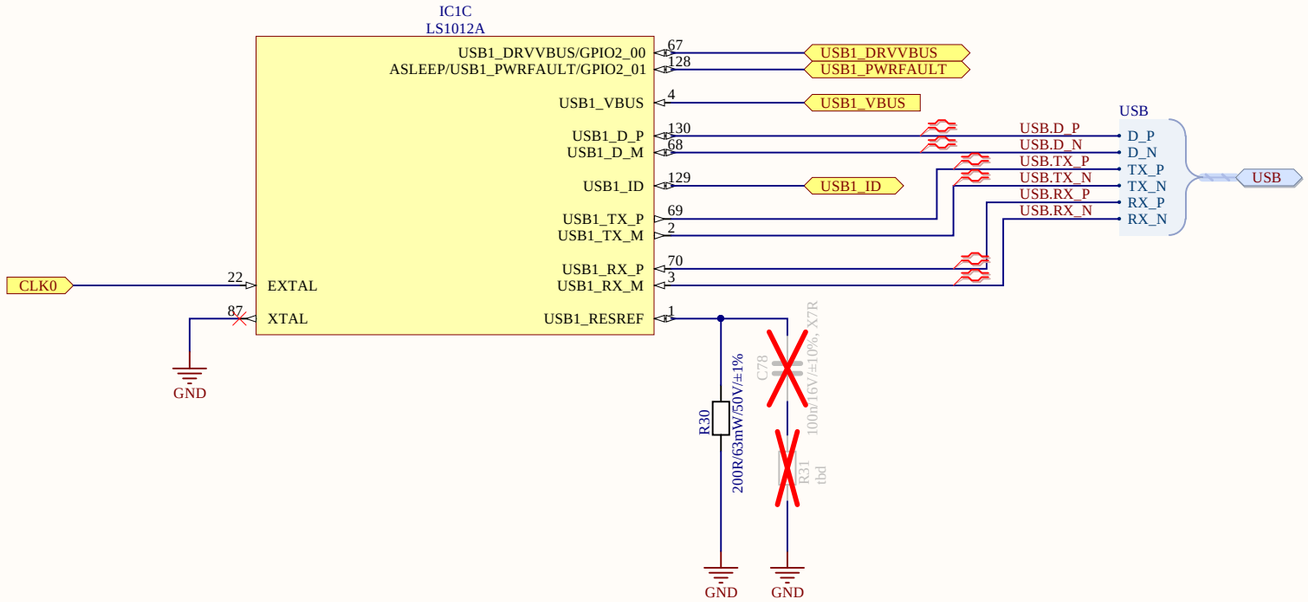

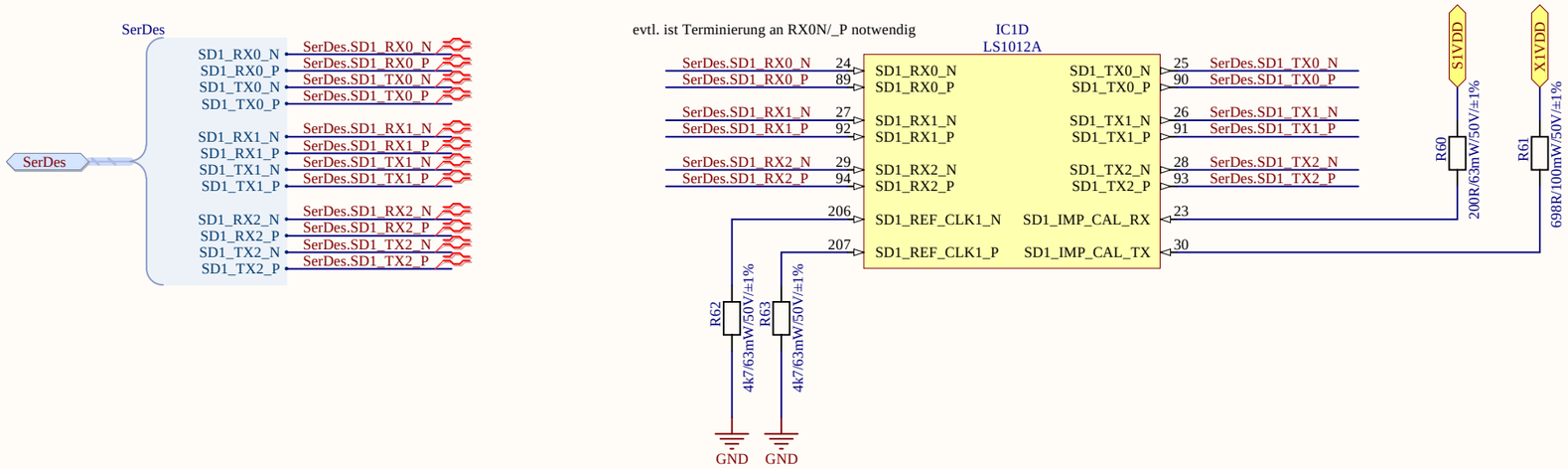

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Document:	LS1012A_USB3.0_SerDes.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
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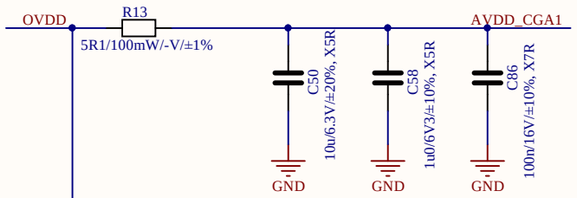
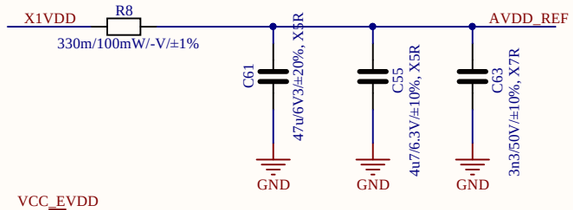
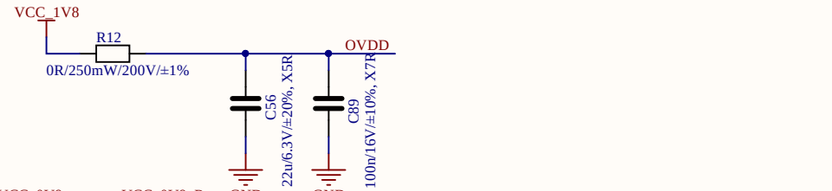
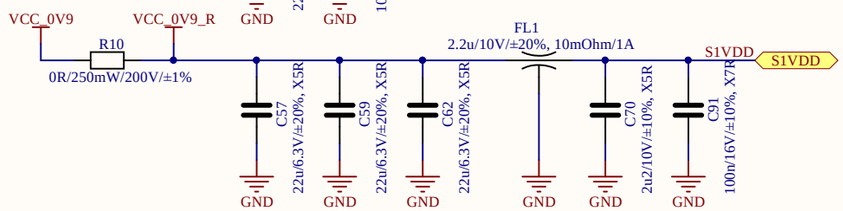
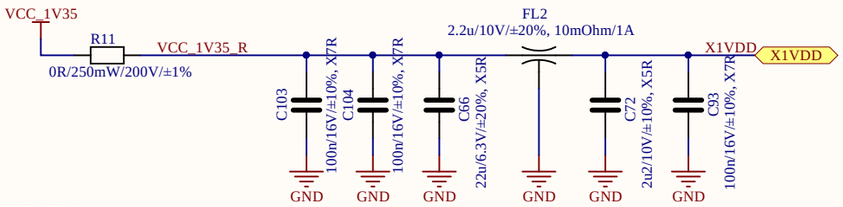
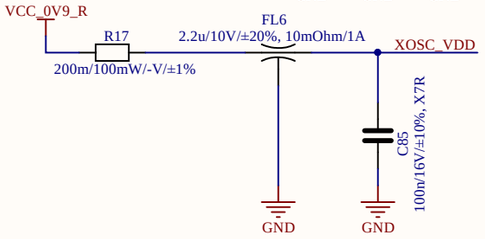


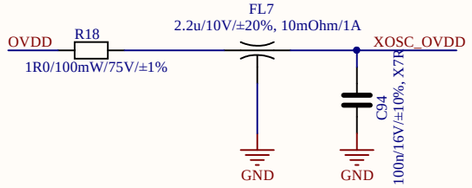


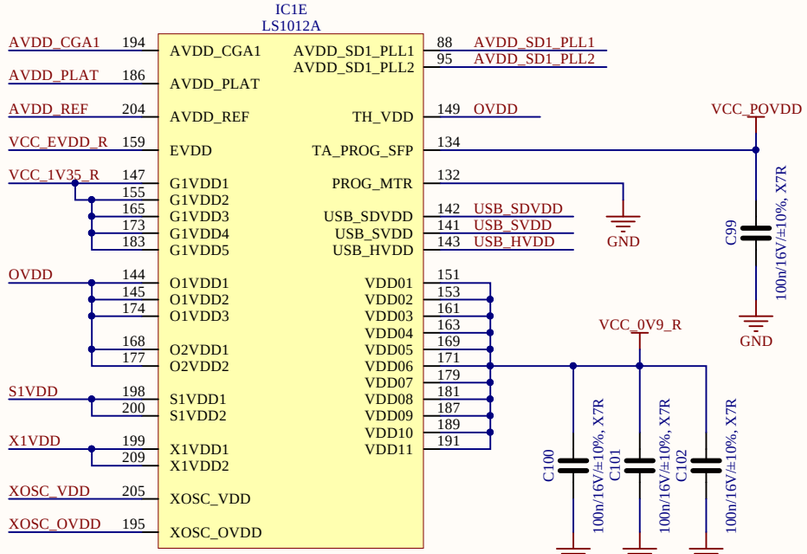


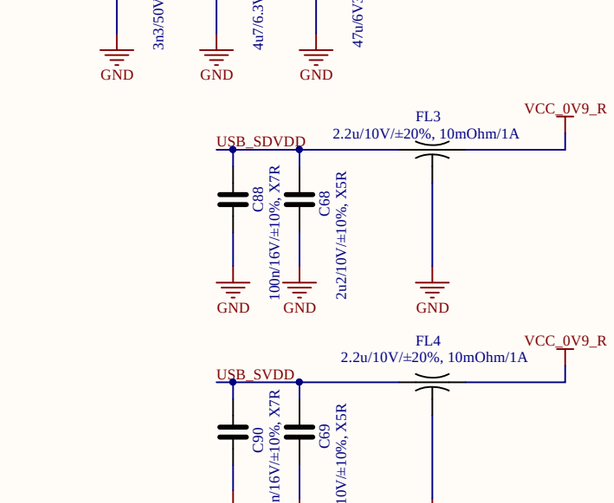


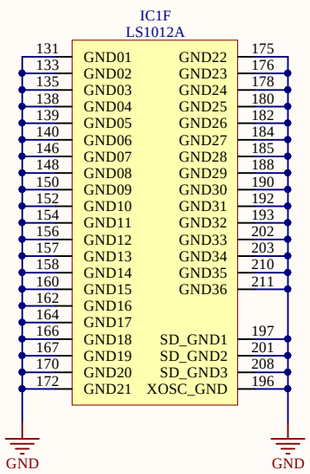


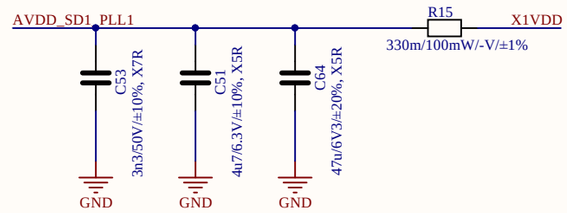


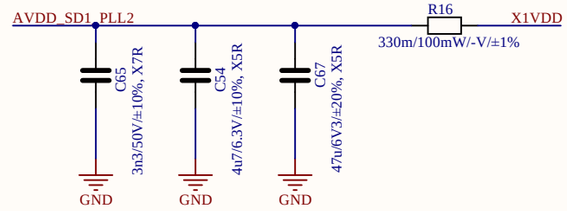




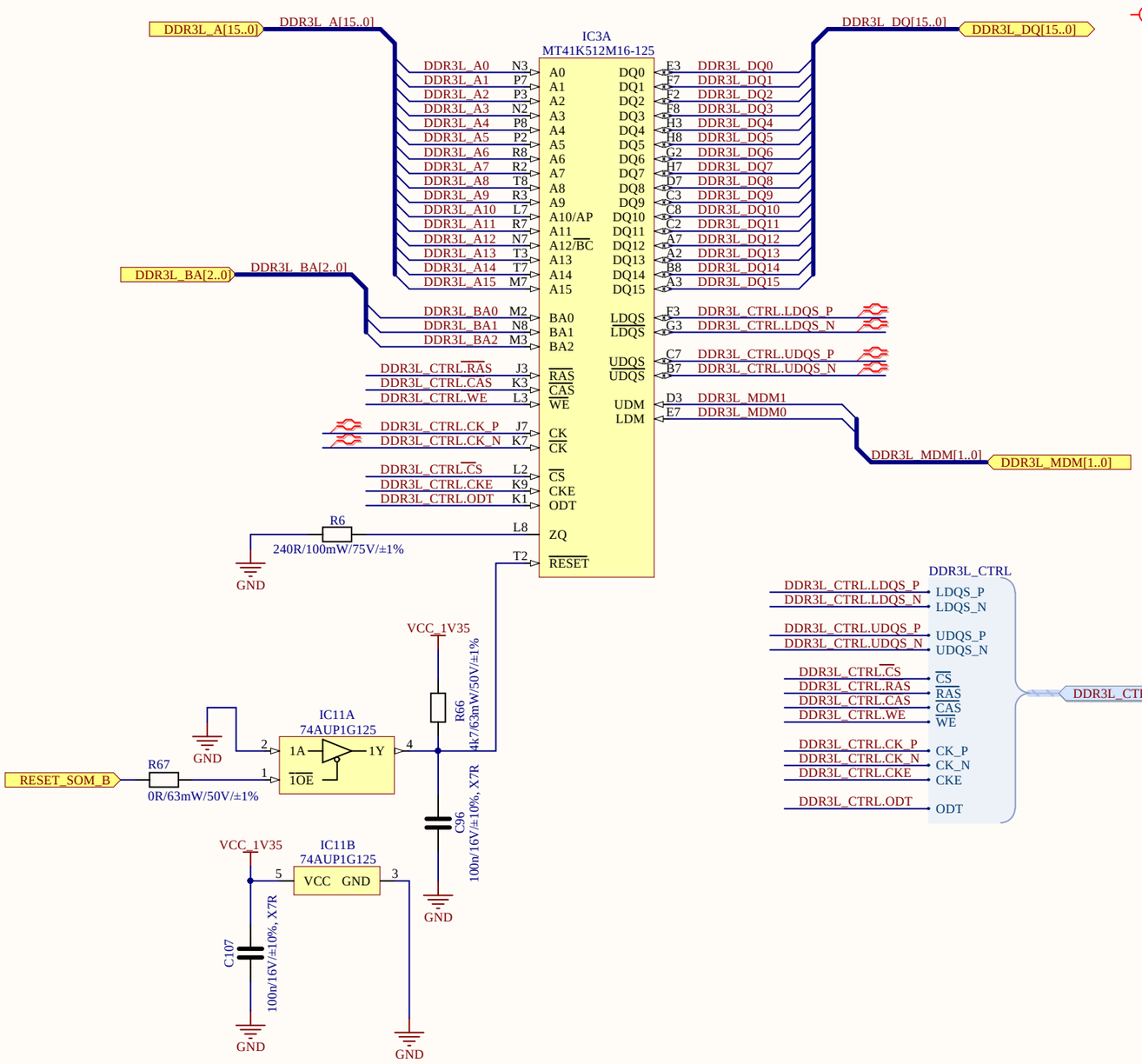








Schematics		SYSTART GmbH	
Project: SaM-Board1012_V200.PrjPcb			
Document:	LS1012A_Spannungsversorgung.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
Status:	Confirmed	Page:	6



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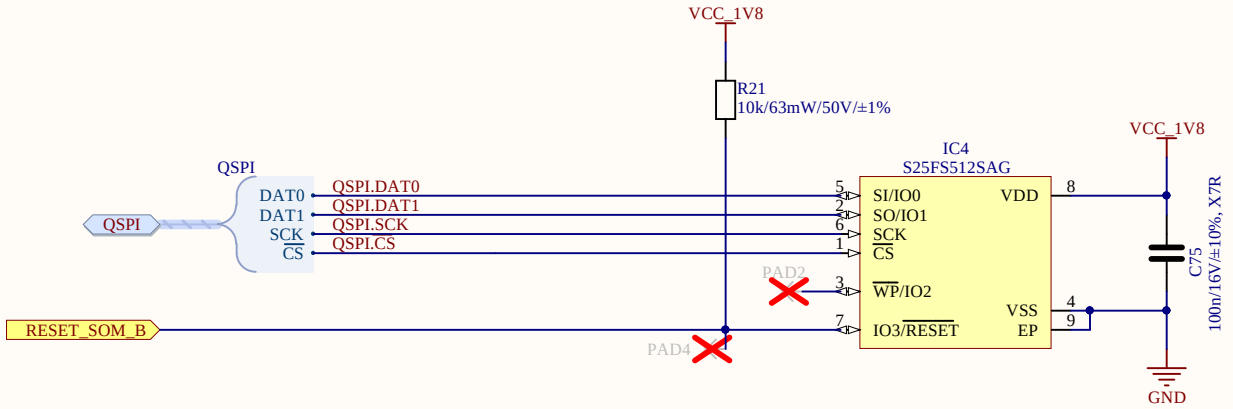
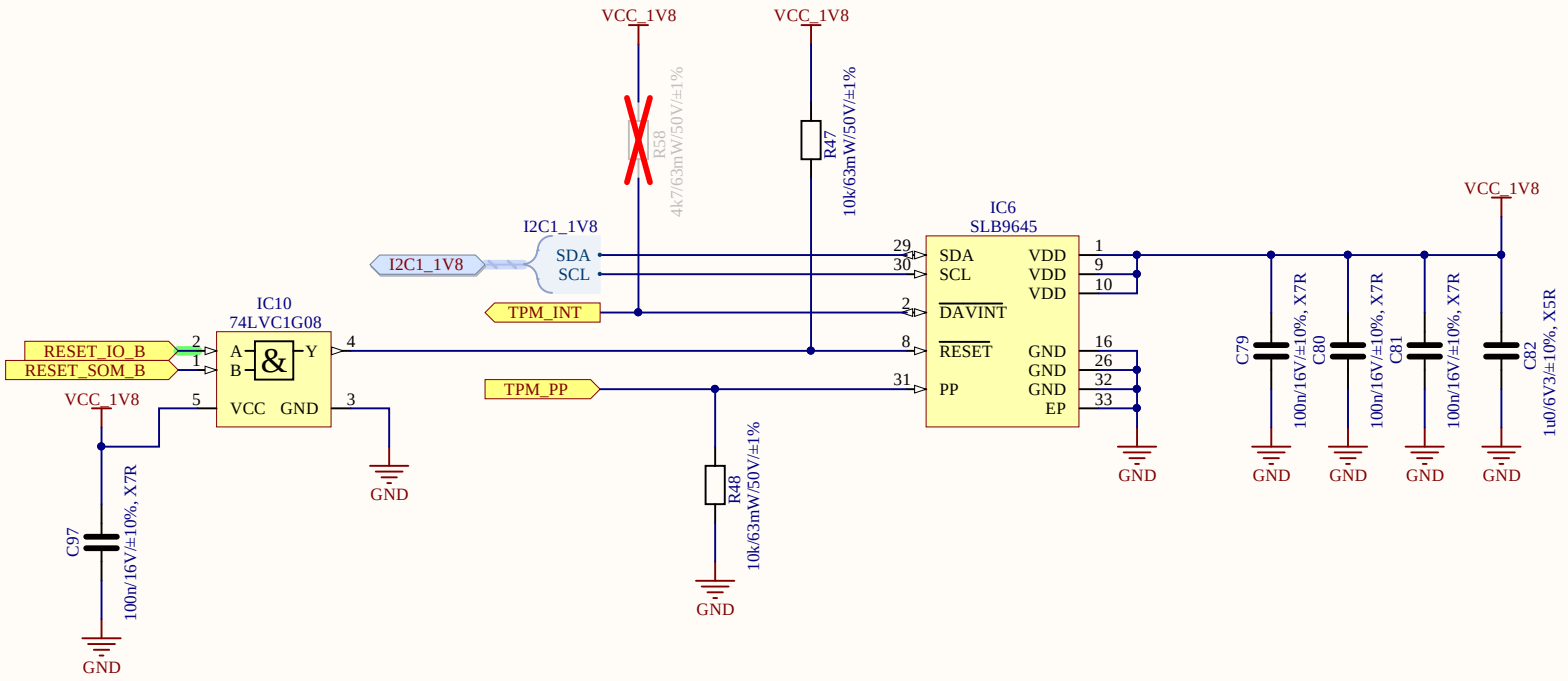
Project: SaM-Board1012_V200.PrjPcb			
Document:	DDR3L.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
Status:	Confirmed	Page:	7

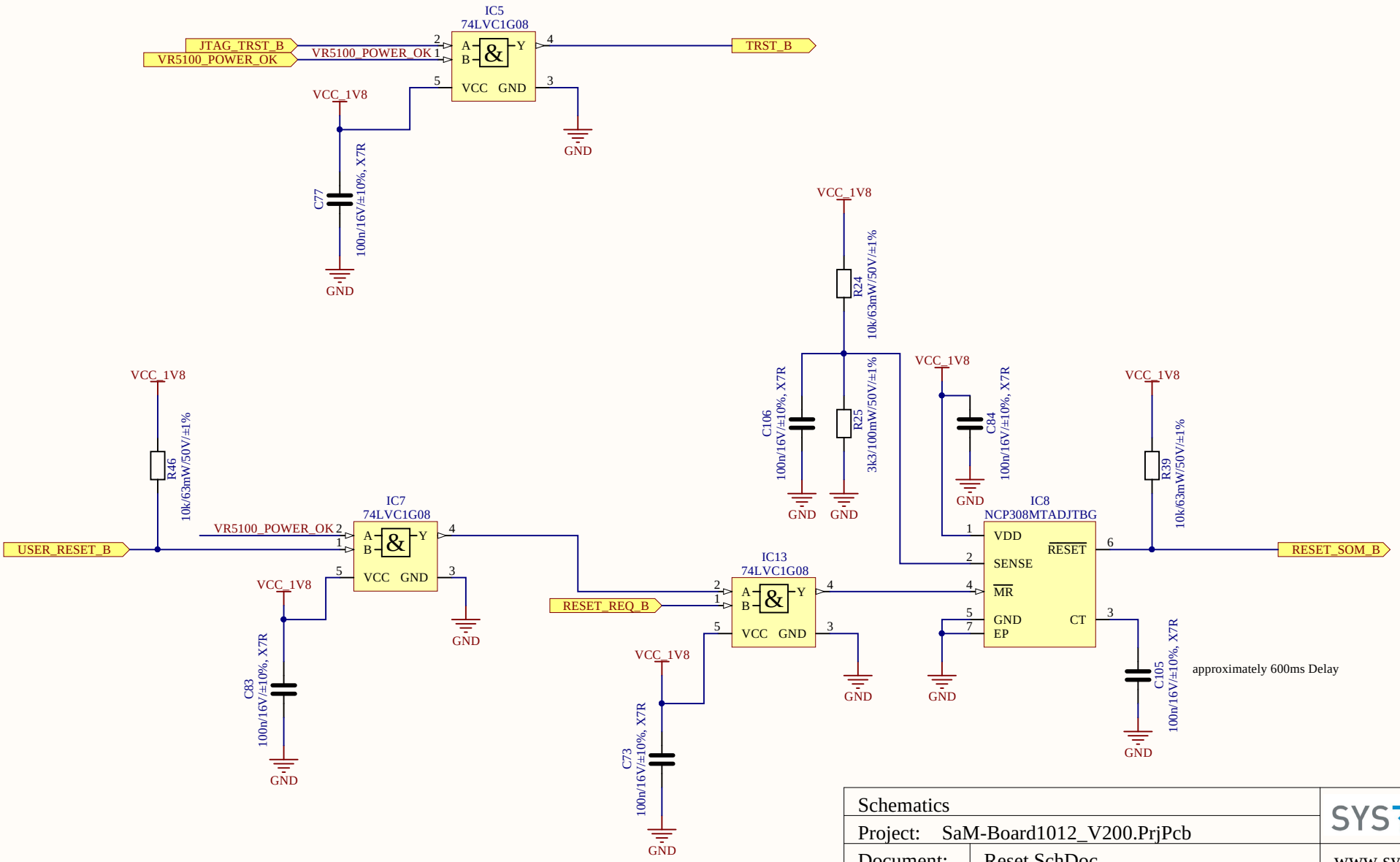


WPn/IO2:
The signal has an internal pull-up resistor and

Schematics		SYSTART GmbH	
Project: SaM-Board1012_V200.PrjPcb			
Document:	QSPI-Flash.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
Status:	Confirmed	Page:	8



Schematics		SYSTART GmbH	
Project: SaM-Board1012_V200.PrjPcb			
Document:	TPM-Modul.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
Status:	Confirmed	Page:	9



Schematics		SYSTART GmbH	
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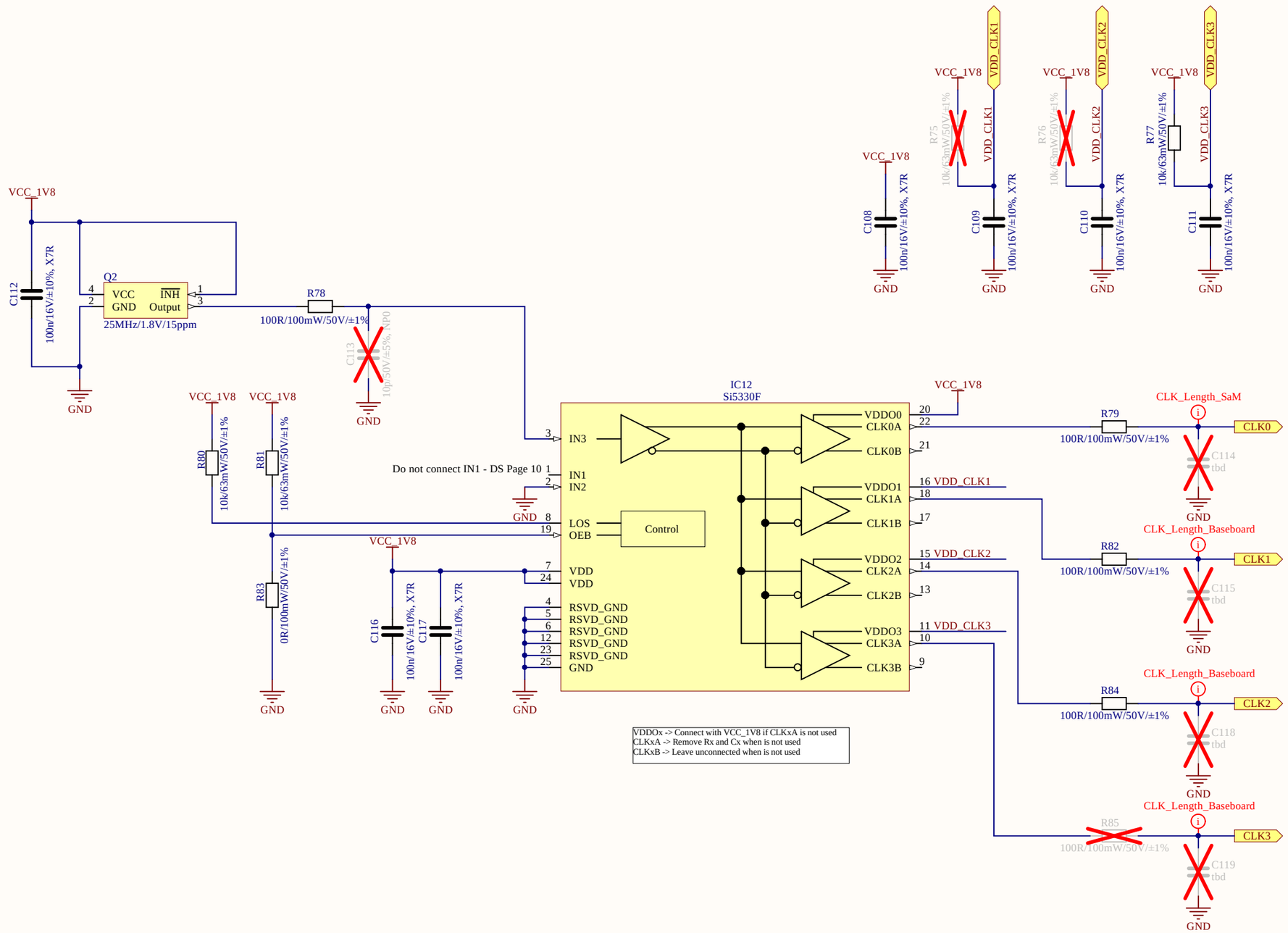
Document:	Reset.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
Status:	Confirmed	Page:	10



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Document:	ClockBuffer.SchDoc	www.systart.de	
Author:	SAM	Date:	17.11.2017
Auditor:	MSB	Date:	18.11.2017
Status:	Confirmed	Page:	11